REMARKS

Claims 1, 7, and 12 are currently pending in the present application, with Claims 1 and 12 being amended and Claim 11 being canceled. Reconsideration and reexamination of the claims are respectfully requested.

The Examiner objected to the disclosure due to various informalities, each of which is addressed below:

The Examiner noted that reference labels (2, 3, 4) need to be described with respect to Fig. 1 as amended. Applicant respectfully point the Examiner's attention to Applicants' previous communication, filed on June 12, 2003, in which Applicants have already amended the specification to include such description.

The Examiner objected to the disclosure for the lack of description to reference labels (16^{IV}, 16^{V}, 16^{VI}) relative to Fig. 5. Applicants respectfully point the Examiner's attention to page 6, line 6 of the specification, in which "conductive strips 16', 16'', 16''' . . . 16^{N}, where N is an odd integer" are referenced. Applicants respectfully submit that labels 16^{IV}, 16^{V}, 16^{VI} are in fact referenced by the series and hence no amendment to the specification is necessary.

The Examiner indicated that label 10 still needs to be added to the drawing. Applicants have already responded to this objection in the previous communication, and repeat Applicants' previous response:

> Applicants respectfully disagrees with the Examiner in that conductive layers 10, which are separated by nonconductive separator layers 20, are not shown in Fig. 6. Rather, Fig. 6 shows the arrangements of the conductive strips (16', 16'', and 16''') and the vias 22. Accordingly, label 10 should not be added to Fig. 6.

The Examiner rejected Claims 1 and 7 under 35 U.S.C. § 102(b) as being anticipated by Landis. This rejection is respectfully traversed with respect to the amended claims.

Amended Claim is directed to on-chip transmission line within the environment of an integrated chip having circuit elements (such as transistors, capacitors, resistors, etc.), whereby the monolithic transmission line includes multiple layers of alternating conductive layers and

nonconductive layers, and whereby the top and bottom conductive layers have a uniform distance from each other, and substantially equals to the distance between the two laterally spaced terminal conductive strips.

Landis does not contain any disclosure or suggestion of an on-chip monolithic transmission line within an environment of integrated circuit having circuit elements. Again, Figs. 1 and 3 of Landis simply show conductive strips that are embedded on a circuit board whereby chips mounted on the boards can be connected to each other via the board-embedded transmission lines via wires 64 and 66. Although Fig. 3 shows two integrated circuit chips, Landis does not show the on-chip transmission lines WITHIN the environment of an integrated circuit chip for interconnecting between different circuit elements. The Examiner noted in the Detailed Action that Claims 1 does not recite any "circuit elements" to claim this aspect of the invention. Applicants have amended Claim 1 to further clarify that the on-chip transmission line claimed exists as a part of an integrated circuit chip, not a circuit board. Accordingly, Applicants respectfully submit that Claims 1 and 7 are not anticipated by, nor obvious in view of, Landis.

The Examiner rejected Claim 11 under 35 U.S.C. § 103(a) as being unpatentable over Landis. This rejection is respectfully traversed with respect to the amended claim. This rejection is moot in view of the canceled claim.

The Examiner objected to Claim 12 as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. Applicants have amended Claim 12 to include all of the limitations of canceled Claim 11 and respectfully submit that amended Claim 12 is in condition for allowance.

In view of the foregoing, Applicants respectfully submit that all of the pending claims are in condition for allowance. An entry of the claim amendments after final is requested. Reconsideration and reexamination of the claims and an early allowance is solicited. If the Examiner believes it would further advance the prosecution of the present application, he is respectfully requested to contact the undersigned attorney.

In the unlikely event that the transmittal letter is separated from this document and the Patent Office determines that an extension and/or other relief is required, Applicant(s) petition(s) for any required relief including extensions of time and authorizes the Assistant Commissioner to charge the cost of such petitions and/or other fees due in connection with the filing of this document to **Deposit Account No. 03-1952** referencing docket no. 53535.20005.00.

Respectfully submitted,

Dated: November 7, 2003 By: _____

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